IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 – 49. (Cancelled)

50. (Original) A controller for an ultra-wideband (UWB) network node, the controller comprising:

a processor having a processor control bus and a processor data bus;

processor memory coupled to said processor data bus;

buffer memory coupled to a second data bus;

a memory access controller coupled to said second data bus and to said processor control bus; and

a UWB interface for interfacing to a UWB communications device, coupled to said processor control bus and to said second data bus; and

wherein said processor is master of said processor control bus and said memory access controller is master of said second data bus.

51 – 60. (Cancelled)

61. (New) The controller of claim 50, wherein the processor memory includes program memory and/or data memory.

62. (New) The controller of claim 50 further comprising a second interface coupled to said processor control bus and to said second data bus.

63. (New) The controller of claim 50, wherein the UWB communications device performs forward error correction.

64. (New) The controller of claim 62, wherein the second interface includes at least one of: a PCI interface, an Ethernet interface, or a second UWB interface.

65. (New) The controller of claim 62, wherein the second interface interfaces to a host processor associated with at least one of: a television, a computer, or a set top box.

66. (New) The controller of claim 50, wherein the buffer memory is used to buffer transmitted packet data.

67. (New) The controller of claim 61, wherein the memory access controller is configured to move packet header data from the buffer memory to the data memory.

68. (New) The controller of claim 50, wherein the memory access controller includes a plurality of registers accessible to the processor via the processor control bus.

69. (New) The controller of claim 68, wherein the plurality of registers is used to store packet control information.

70. (New) The controller of claim 69, wherein the packet control information includes channel handle information.

71. (New) The controller of claim 50 further comprising additional memory appended to the buffer memory.

72. (New) The controller of claim 50, wherein the additional memory includes at least one of: flash memory or SDRAM.